

Abstract

A digital true random number generator circuit, comprising
a linear feedback shift register having an input and an output, a system
clock having a system clock frequency value for driving the shift
register, and a plurality of free running oscillators operatively
connected to the input of the shift register. The oscillators and the
system clock having different oscillation frequency values, the greatest
common divisor of which having the value one, thereby avoiding locking of
the oscillators and the system clock.